Amendments to the Claims:

Please amend the claims as follows:

1. (Currently amended) An insulated gate type semiconductor device comprising:

a body region arranged at upper surface side in a semiconductor substrate, the body region having ~~corresponding to~~ a first conductive ~~conduction~~ type semiconductor;

a drift region being in contact with bottom surface of the body region, the drift region having ~~corresponding to~~ a second conductive ~~conduction~~ type semiconductor; and

a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region,

wherein the insulated gate type semiconductor further comprises a floating region surrounded by the drift region, the floating region having ~~corresponding to~~ a first conductive ~~conduction~~ type semiconductor,

bottom of the trench section is arranged in the floating region,

in the trench section, there are formed a deposited insulating layer consisting of deposited insulating material and a gate electrode being arranged above the deposited insulating layer and facing the body region, and

~~top of the deposited insulating layer~~ a lower end of the gate electrode is further above top of the floating region,

a space between the bottom surface of the body region and the top of the floating region is wider than a space between a lower end of the deposited insulating layer and a lower end of the floating region, and

a space between the lower end of the gate electrode and the lower end of the deposited insulating layer is wider than a space between the bottom surface of the body region and the top of the floating region.

2. (Currently amended) An insulted gate type semiconductor device according to claim 1 further comprising an intermediate floating region

arranged further above top of the floating region with being surrounded by the drift region, the intermediate floating region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor,

wherein the trench section penetrates the intermediate floating region, and

top of the deposited insulating layer is arranged further above top of the intermediate floating region.

3. (Currently amended) An insulated gate type semiconductor device according to claim 1 further comprising:

an auxiliary trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the auxiliary trench section being filled with insulating material inside; and

an auxiliary floating region surrounded by the drift region, the auxiliary floating region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor,

wherein bottom of the auxiliary trench section is arranged in the auxiliary floating region.

4. (Original) An insulated gate type semiconductor device according to claim 3 wherein depth of the trench section and depth of the auxiliary trench section are different.

5. (Original) An insulated gate type semiconductor device according to claim 3 wherein depth of the trench section and depth of the auxiliary trench section are same.

6. (Currently amended) An insulated gate type semiconductor device comprising:

a body region arranged at upper surface side in a semiconductor substrate, the body region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor;

a drift region being in contact with bottom surface of the body region,

the drift region ~~corresponding to~~ having a second ~~conduction~~ conductive type semiconductor;

a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region; and

a gate electrode arranged in the trench section with facing the body region,

wherein the insulated gate type semiconductor device further comprises:

an auxiliary trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the auxiliary trench section being filled with insulating material inside; and

an auxiliary floating region surrounded by the drift region, the auxiliary floating region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor,

wherein bottom of the auxiliary trench section is arranged in the auxiliary floating region, and

a space between the bottom surface of the body region and the top of the auxiliary floating region is wider than a space between a lower end of the deposited insulating layer and a lower end of the auxiliary floating region.

7. (Currently amended) An insulated gate type semiconductor device according to claim 6 further comprising an auxiliary intermediate floating region arranged further above top of the auxiliary floating region with being surrounded by the drift region, the auxiliary intermediate floating region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor,

wherein the auxiliary trench section penetrates the auxiliary intermediate floating region, and

top of the deposited insulating layer is arranged further above top of the auxiliary intermediate floating region.

8. (Currently amended) An insulated gate type semiconductor device according to claim 6 further comprising:

a second auxiliary trench section facing the auxiliary trench section with the gate electrode inserted between there, the second auxiliary trench section being arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the second auxiliary trench section being filled with insulating material inside; and

a second auxiliary floating region surrounded by the drift region, the second auxiliary floating region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor,

wherein depth of the auxiliary trench section and depth of the second auxiliary trench section are different.

9. (Currently amended) An insulated gate type semiconductor device according to claim 3 [[or 6]], wherein the auxiliary trench section is structure in dot pattern, viewed from top side of the semiconductor substrate.

10. (Currently amended) An insulated gate type semiconductor device according to ~~at least any one of claims 1 through 9~~ claim 1,

wherein in a region around a cell region, there are arranged:

a terminal trench section filed with insulating material inside; and

a terminal floating region surrounded by the drift region, the terminal floating region ~~corresponding to~~ having a first conductive type semiconductor, and

bottom of the terminal trench section is arranged in the terminal floating region, and

a space between adjoining terminal floating regions is narrower than a space between the bottom surface of the body region and a top of the terminal floating region.

11. (Currently amended) Manufacturing method of an insulated gate type semiconductor device which comprises:

a body region arranged at upper surface side in a semiconductor substrate, the body region ~~corresponding to~~ having a first ~~conduction~~ conductive type semiconductor; a drift region being in contact with bottom

surface of the body region, the drift region ~~corresponding to~~ having a second ~~conduction~~ conductive type semiconductor; a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region; and a gate electrode arranged in the trench section with facing the body region, the manufacturing method further comprising:

trench section forming step of forming the trench section in the semiconductor substrate on which the drift region and the body regions have been formed;

oxide film forming step of forming an oxide film on a side wall of the trench section formed in the trench section forming step;

impurity injecting step of, after formation of the oxide film in the oxide film forming step, injecting impurity from bottom of a trench section formed in the trench section forming step;

insulating material laying-up step of laying up insulating material in the trench section after impurity is injected through the impurity injecting step; and

floating region forming step of forming a floating region by applying thermal diffusion processing after ~~impurity is injected~~, the insulating material is laid up in the insulating material laying-up step.

12. (Original) Manufacturing method of an insulated gate type semiconductor device according to claim 11 further comprising:

trench section drilling step of further drilling down bottom of the trench section after impurity is injected in the impurity injecting step; and

impurity re-injecting step of re-injecting impurity from bottom the trench section drilled further in the trench section drilling step.

13. (Currently amended) Manufacturing method of an insulated gate type semiconductor device according to claim 11 ~~or 12~~, wherein

the trench section is formed in a cell region and a ~~peripheral~~ region [[of]] around the cell region in the trench section forming step, and

the insulating material laying-up step comprises:

insulating material filling step of filling inside of the trench section

formed in the trench section forming step with insulating material; and

deposited material adjusting step of adjusting height of a deposited insulating layer by eliminating a portion of insulating material in the trench section filled with insulating material in the insulating material filling step, particularly, the trench section in the cell region.

14. (New) An insulated gate type semiconductor device according to claim 1, wherein

a thickness of the deposited insulating layer is a thickness enough to form peaks of electric field at two positions in a direction of thickness of the semiconductor substrate.

15. (New) An insulated gate type semiconductor device according to claim 6, wherein

a depth of the auxiliary trench section is a depth enough to form peaks of electric field at two positions in a direction of thickness of the semiconductor substrate.

16. (New) An insulated gate type semiconductor device according to claim 1, wherein

the lower end of the gate electrode and the bottom surface of the body region are substantially the same in depth.

17. (New) An insulated gate type semiconductor device according to claim 1, wherein

the floating region has a nearly circular shape in section.

18. (New) Manufacturing method of an insulated gate type semiconductor device according to claim 11 further comprising:

etching-back step of removing part of the insulating material by a depth substantially equal to the bottom surface of the body region after the insulating material is laid up in the insulating material laying-up step; and

gate material laying-up step of laying up a gate material in a space

formed in the trench section in the etching-back step.

19. (New) An insulated gate type semiconductor device according to claim 6, wherein the auxiliary trench section is structure in dot pattern, viewed from top side of the semiconductor substrate.

20. (New) An insulated gate type semiconductor device according to claim 6,

wherein in a region around a cell region, there are arranged:

a terminal trench section filed with insulating material inside; and

a terminal floating region surrounded by the drift region, the terminal floating region having a first conductive type semiconductor, and

bottom of the terminal trench section is arranged in the terminal floating region, and

a space between adjoining terminal floating regions is narrower than a space between the bottom surface of the body region and a top of the terminal floating region.

21. (New) An insulated gate type semiconductor device according to claim 6, wherein

the lower end of the gate electrode and the bottom surface of the body region are substantially the same in depth.

22. (New) An insulated gate type semiconductor device according to claim 6, wherein

the floating region has a nearly circular shape in section.